# On Circuit Diameter Bounds via Circuit Imbalances 

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## Overview

(1) Diameter and Circuit Diameter of Polyhedra
(2) Circuit Imbalance Measure $\kappa$
(3) Main Results:

- Circuit diameter bounds in terms of $\kappa$
- Circuit augmentation algorithms for LP (runtime in terms of $\kappa$ )
(4) Conclusion and Future Directions


## Linear Programming

- Given $A \in \mathbb{R}^{m \times n}, b \in \mathbb{R}^{m}, c \in \mathbb{R}^{n}$,

$$
\begin{array}{lll}
\text { (Primal) } \begin{array}{ll}
\min c^{\top} x & \text { (Dual) } \\
\text { s.t. } A x=b & \\
& \text { max } b^{\top} y \\
& \text { s.t. } A^{\top} y \\
&
\end{array} .
\end{array}
$$



- $n$ variables, $m$ constraints, $L_{A, b, c}$ encoding length of the input
- Ellipsoid and Interior Point Methods run in poly ( $n, m, L_{A, b, c}$ ) time.
- For Simplex Method, no polynomial pivot rule is known.

Smale's 9th Question: Is there a strongly polynomial algorithm for LP? (runs in poly $(n, m)$ arithmetic operations using poly ( $n, m, L_{A, b, c}$ ) space.)

## Simplex Method and Diameter

- Consider the polyhedron

$$
P=\{x: A x=b, x \geq 0\} .
$$

- The diameter of $P$ is the max \# of edges in a shortest path between any 2 vertices.
- Diameter $\leq \#$ of simplex pivots.

Hirsch's Conjecture: The diameter of a $d$-dimensional polyhedron with $f$ facets is $\leq f-d$.

- Disproved by Santos in 2012.
- Polynomial version $(\leq p o l y(f))$ is still open.
- Quasi-polynomial upper bound known [Kalai-Kleitman '92], [Todd '14]. Current best bound: $(f-d)^{\log O(d / \log d)}$ [Sukegawa '18].


## Circuit Diameter

- For $W=\operatorname{ker}(A), g \in W \backslash\{0\}$ is a circuit if $\nexists h \in W \backslash\{0\}$ such that

$$
\operatorname{supp}(h) \subsetneq \operatorname{supp}(g)
$$

- Circuits are all possible edge directions of $P$ when varying $b$.
- A circuit walk is a sequence of points $x^{(1)}, x^{(2)}, \ldots, x^{(k)}$ in $P$ where $x^{(t+1)}$ is obtained from $x^{(t)}$ by moving along a circuit maximally.
- The circuit diameter of $P$ is the max \# of steps in a shortest circuit walk between any 2 vertices.
- Circuit diameter $\leq$ diameter.


Circuit Hirsch's Conjecture [Borgwardt, Finhold, Hemmecke '15]: The circuit diameter of a $d$-dimensional polyhedron with $f$ facets is $\leq f-d$.

## Goals

(1) Upper bound the circuit diameter of $P$.
(2) Give an efficient circuit augmentation algorithm for solving

$$
\min \left\{c^{\top} x: x \in P\right\}
$$

## State of the Art

- Circuit diameter of combinatorial polyhedra:
- Dual transportation polyhedra [Borgwardt, Finhold, Hemmecke '15].
- Matching, travelling salesman and fractional stable set polytopes [Kafer, Pashkovich, Sanità '19].
- Circuit augmentation algorithms in network flow:
- Edmonds-Karp-Dinic algorithm for max flow.
- Min-mean cycle canceling for min-cost flow [Goldberg-Tarjan '89].
- Min-ratio cycle canceling for min-cost flow [Wallacher '89].
- All extended to LP [Bland '76], [Gauthier-Desrosiers '21], [Ekbatani, Natura, Végh '21], [McCormick-Shioura '00].
- Other circuit augmentation rules [De Loera, Hemmecke, Lee '15].
- Circuit augmentation on 0/1-polytopes [De Loera, Kafer, Sanità '19].


## Circuit Imbalance Measure

- For $W=\operatorname{ker}(A)$, the circuit imbalance measure is

$$
\kappa_{W}=\max \left\{\left|\frac{g_{i}}{g_{j}}\right|: i, j \in \operatorname{supp}(g), g \text { circuit in } W\right\} .
$$

- $\kappa_{W}=\kappa_{W \perp}$.
- If $A$ is totally unimodular, then $\kappa_{W}=1$.

- For integral $A$ with max subdeterminant $\Delta$, $\kappa_{W} \leq \Delta$.
- E.g., if $A$ is the incidence matrix of $K_{n}$,
 then $\kappa_{W} \leq 2$ and $2^{\lfloor n / 3\rfloor} \leq \Delta$ because

$$
\operatorname{det}\left(\begin{array}{lll}
1 & 1 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1
\end{array}\right)=2
$$



## Circuit Diameter Bounds

## Theorem 1 (Uncapacitated)

For $A \in \mathbb{R}^{m \times n}$ and $b \in \mathbb{R}^{m}$, the circuit diameter of

$$
P=\{x: A x=b, x \geq 0\}
$$

is $O\left(m^{2} \log (m+\kappa W)\right)$.

## Theorem 2 (Capacitated)

For $A \in \mathbb{R}^{m \times n}, b \in \mathbb{R}^{m}$ and $u \in \mathbb{R}^{n}$, the circuit diameter of

$$
P_{u}=\{x: A x=b, 0 \leq x \leq u\}
$$

is $O\left(m^{2} \log (m+\kappa w)+n \log n\right)$.

Note: Simple reduction from $P_{u}$ to $P$ only gives $O\left(n^{2} \log (n+\kappa w)\right)$.

## Uncapacitated Circuit Diameter

- Let $P=\{x: A x=b, x \geq 0\}$ and $W=\operatorname{ker}(A)$.
- Every $x \in W$ can be decomposed into $\leq n$ conformal circuits $g^{(i)} \in W$ :

$$
x=\sum_{i=1}^{k} g^{(i)}
$$

such that $\operatorname{sgn}\left(g_{j}^{(i)}\right)=\operatorname{sgn}\left(x_{j}\right)$ for all $i \in[k]$ and $j \in[n]$.
Idea: Given vertices $x, y \in P$, let $B$ be a basis for $y$ and $N:=[n] \backslash B$.

- Decompose $y-x$ into conformal circuits $g^{(1)}, g^{(2)}, \ldots, g^{(k)}$.
- Pick $g^{(i)}$ with the largest $\left\|g_{N}^{(i)}\right\|_{1}$ and augment.
- Repeat.



## Proof of the $O\left(m^{2} \log \left(m+\kappa_{W}\right)\right)$ bound

- Let $x^{(0)}, x^{(1)}, \ldots$ be the resulting circuit walk from $x$ to $y$.

Geometric decay: $\left\|x_{N}^{(t+1)}\right\|_{1} \leq\left(1-\frac{1}{n}\right)\left\|x_{N}^{(t)}\right\|_{1}$

- We analyze the sets

$$
L_{t}=\left\{i \in[n]: y_{i}>n \kappa_{W}\left\|x_{N}^{(t)}\right\|_{1}\right\} \quad R_{t}=\left\{i \in[n]: x_{i}^{(t)} \leq n y_{i}\right\}
$$



## Proof of the $O\left(m^{2} \log \left(m+\kappa_{W}\right)\right)$ bound

$$
L_{t}=\left\{i \in[n]: y_{i}>n \kappa w\left\|x_{N}^{(t)}\right\|_{1}\right\} \quad R_{t}=\left\{i \in[n]: x_{i}^{(t)} \leq n y_{i}\right\}
$$



Lemma 1: $L_{t} \subseteq L_{t+1} \subseteq B$ and $R_{t} \subseteq R_{t+1}$.
Lemma 2: $L_{t}$ or $R_{t}$ grows in $O\left(n \log \left(n+\kappa_{W}\right)\right)$ iterations.
$\Longrightarrow$ Circuit diameter $O\left(n^{2} \log (n+\kappa W)\right)$. How to turn $n$ into $m$ ?

## Capacitated Circuit Diameter

- Let $P_{u}=\{x: A x=b, 0 \leq x \leq u\}$.
- First, augment using conformal circuits of $y-x^{(t)}$ which minimize an auxiliary cost function.
- Then, remove $n-m$ capacity constraints using the following subroutine:


## Support-Circuit (a.k.a. Moving to a face)

Input: Feasible point $x \in P_{u}$
Output: A circuit $z \in \operatorname{ker}(A)$ where $\operatorname{supp}(z) \subseteq \operatorname{supp}(x)$.

- Finally, reduce to uncapacitated form and apply Theorem 1.

$$
\left\{(x, s):\left[\begin{array}{cc}
A & 0 \\
I_{m} & I_{m}
\end{array}\right]\left[\begin{array}{l}
x \\
s
\end{array}\right]=\left[\begin{array}{l}
b \\
u
\end{array}\right],(x, s) \geq 0\right\}
$$

## Circuit Augmentation Algorithms

- Recall $P=\{x: A x=b, x \geq 0\}$. We use the following subroutine:


## Ratio-Circuit (Wallacher's Rule)

Input: Cost $c \in \mathbb{R}^{n}$ and feasible point $x \in P$.
Output: A circuit $z \in \operatorname{ker}(A)$ such that $z_{[n] \backslash \operatorname{supp}(x)} \geq 0$ and minimizes

$$
\frac{c^{\top} z}{\sum_{i \in \operatorname{supp}(x)} \frac{\max \left(-z_{i}, 0\right)}{x_{i}}}
$$

Geometric decay: Augmenting along $z$ shrinks the optimality gap by a factor of $\left(1-\frac{1}{n}\right)$.
$\Longrightarrow$ Weakly polynomial but not finite!

## Circuit Augmentation Algorithms

## Theorem 3 (Feasibility)

There is a circuit augmentation algorithm which given $N \subseteq[n]$ finds

$$
x \in P \text { such that } x_{N}=0,
$$

or a dual certificate showing that no such solution exists, using $O\left(n^{2} \log \left(n+\kappa_{W}\right)\right)$ Ratio-Circuit and $n^{2}$ Support-Circuit calls.

## Theorem 4 (Optimization)

There is a circuit augmentation algorithm which solves

$$
\min \left\{c^{\top} x: x \in P\right\}
$$

using $O\left(n^{3} \log (n+\kappa w)\right)$ Ratio-Circuit and $n^{3}$ Support-Circuit calls.

- How does this differ to the circuit diameter setting?


## Conclusion

For $\min \left\{c^{\top} x: A x=b, x \geq 0\right\}$ where $A \in \mathbb{R}^{m \times n}$,

## Summary of Results:

(1) Circuit diameter bounds:

- $O\left(m^{2} \log \left(\kappa_{W}+m\right)\right)$ for uncapacitated.
- $O\left(m^{2} \log \left(\kappa_{W}+m\right)+n \log n\right)$ for capacitated.
(2) Circuit augmentation algorithms:
- $O\left(n^{2} \log (\kappa w+n)\right)$ Ratio-Circuit and $n^{2}$ Support-Circuit calls for feasibility.
- $O\left(n^{3} \log (\kappa W+n)\right)$ Ratio-Circuit and $n^{3}$ Support-Circuit calls for optimization.


## Open Problems:

(1) poly $\left(n, m, \log \kappa_{W}\right)$ bound on the diameter? poly $\left(n, m, L_{A, b}\right)$ ?

- Current best: $O\left((n-m)^{3} m \kappa_{w} \log \left(\kappa_{w}+n\right)\right)$ [Dadush-Hähnle '16].
(2) poly $(n, m)$ bound on the circuit diameter?

